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A DE-TRIGGERABLE ASTABLE CIRCUIT FOR MICROPROCESSOR RESET.(U)
JAN 82 C B SLINGSBY
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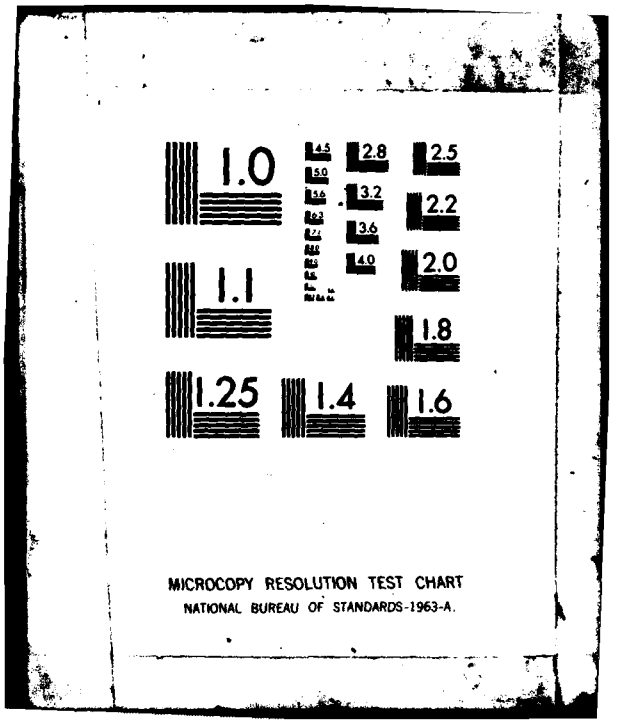
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RSRE
MEMORANDUM No. 3447

ROYAL SIGNALS & RADAR ESTABLISHMENT

A DE-TRIGGERABLE ASTABLE CIRCUIT FOR MICROPROCESSOR RESET

Author: C G Slingsby

PROCUREMENT EXECUTIVE,
MINISTRY OF DEFENCE,
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WORCS.

ROYAL SIGNALS AND RADAR ESTABLISHMENT

Memorandum 3447

Title: A DE-TRIGGERABLE ASTABLE CIRCUIT FOR MICROPROCESSOR RESET

Author: C G Slingsby

Date: January 1982

SUMMARY

A de-triggerable astable circuit is described which has general application for automatic microprocessor system reset. The circuit prevents lock up and program cycle failure which can occur with some reset schemes.

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RSRE MEMORANDUM 3447

A DE-TRIGGERABLE ASTABLE CIRCUIT FOR MICROPROCESSOR RESET

C G Slingsby

LIST OF CONTENTS

1. INTRODUCTION.

This Memorandum describes a circuit which has proved useful for automatic reset of a microprocessor system.

When such a system has power applied, the MPU (microprocessor unit) has to be directed to obey stored instructions, in sequence, starting at a particular point, or location, in such a sequence. To provide this, MPU circuits have a control line normally designated the 'RESET' line, which forces the MPU to a particular memory location containing the initial instruction of a program. The circuit described here automatically effects such a reset if the normal program is not being executed.

2. THEORY

Microprocessor systems commonly use a simple R.C. network to hold the 'reset' line at a logic low level when power is applied. Such a circuit is shown in Fig 1. The time constant of this RC combination is chosen such that the 'reset' line will remain at a low logic level for a suitable length of time (typically 1 - 10mS).

If the power is lost for a short period i.e. a mains transient, the capacitor, C, may not have discharged below the reset voltage threshold value and hence the reset line will not cause the MPU to perform the reset function, although it is very probable that the correct point in the instruction sequence will have been lost.

To eliminate this problem, the reset line should be pulled to a logic low level if the correct sequence of program instructions is not being obeyed. It is virtually impossible in a simple system to monitor the execution of each instruction in sequence but it is quite simple to use the cyclic nature of most program action (calling a particular subroutine, regular interrupt servicing and input/output are examples) to indicate probable correct action.

If such correct program action is considered to produce a pulse stream this could be used to 'inhibit reset'. Unfortunately if this is used directly the system will almost certainly 'lock up'as absence of correct program action will cause the reset line logic level to be held to the reset condition. The MPU, however, will only process instructions after the reset line has been 'released' so the lack of correct program action causes a reset condition which causes no program action.

The solution to this can be provided by the function of a 'de-triggerable astable'.

With no program action, the astable free runs, pulsing the MPU reset line first to the 'reset' logic level then to the 'run' level. The time constant of these pulses is arranged to be considerably longer, e.g. twice, the normal cyclic action of the program. As soon as the program is cycling correctly, pulses will be available to prevent furthur triggering of the astable.

3. CIRCUIT DETAILS

The circuit diagram for a typical 'detriggerable astable' is shown in Fig 2. It uses a common integrated circuit timer with some additional components.

Negative-going pulses are fed through the 7404 inverter and applied to capacitor C2. This capacitor prevents the application of dc from a non-running program causing de-triggering and hence reset inhibition.

The timing capacitor C1 will normally discharge through resistor R1 as pin 7 of the 555 circuit is at a low level while the microprocessor is running. The pulses applied through C2 and D1 will however keep the voltage level 'topped up' and hence prevent the 555 circuit from triggering.

A fuller explanation of the action of a 555 timer is given in Appendix A.

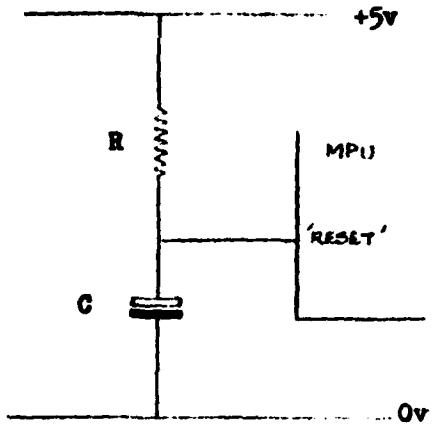
4. CONSTRAINTS

As the circuit is dependant on repeated program action to prevent reset, there may be a few specialised applications where this will not be available. The circuit will be useful in the majority of cases, as even long linear programs normally visit subroutines, service interrupts or perform input/output at regular intervals.

It is also recommended that care be taken during program development as a software error could initiate reset action.

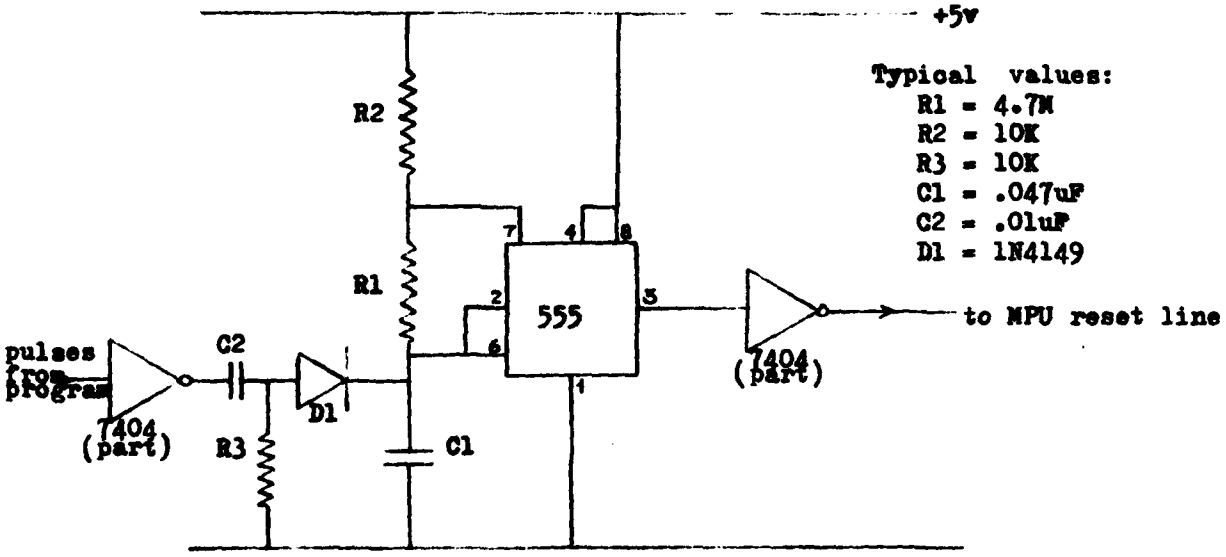
5. CONCLUSION

The de-triggerable astable circuit described in this memorandum has proved most useful for automatic reset of small microprocessor systems, providing a reset function with the ability to respond to incorrect MPU action even if this has been caused by a supply glitch too short to trigger normal RC reset circuits.



Typical values:
R = 1K
C = 1uF

Figure 1. Simple RC reset network



Typical values:
R1 = 4.7M
R2 = 10K
R3 = 10K
C1 = .047uF
C2 = .01uF
D1 = 1N4149

Figure 2. Typical 'de-triggerable' astable circuit.

APPENDIX A

A1. 555 TIMER ACTION (Astable connection)

At switch on, the timing capacitor Ct starts to charge exponentially via the series Rt + Rd1 resistor combination until the capacitor voltage reaches $\frac{2}{3}$ of the voltage rail. At this point the threshold of the 'top' op-amp is reached and its output transition causes the flip-flop to change state. The flip-flop output in turn causes the output stage to provide a '1' output and also internal transistor Q1 to conduct. With this transistor conducting, pin 7 falls to a few hundred millivolts of the ground potential, discharging the capacitor Ct exponentially. The resistor Rd1 limits the current from the +V rail through the discharge pin.

When the voltage on the capacitor Ct has fallen to $\frac{1}{3}$ of the voltage rail, the 'trigger' input, connected to the 'lower' op-amp, causes the flip-flop to again change state, allowing the capacitor Ct to start charging again towards $\frac{2}{3}$ V, thus repeating the cycle.

It may be seen that it is theoretically impossible to get a perfect 1:1 square wave output from this circuit as the '1' output is proportional to K(Rt+Rd1)Ct while the '0' is given by K(Rt)Ct. However, if Rd1 is made small in relation to Rt, a good approximation is obtained.

In the application discussed in this memorandum, a 1:1 astable is not nescessary, the 555 circuit performance is satisfactory.

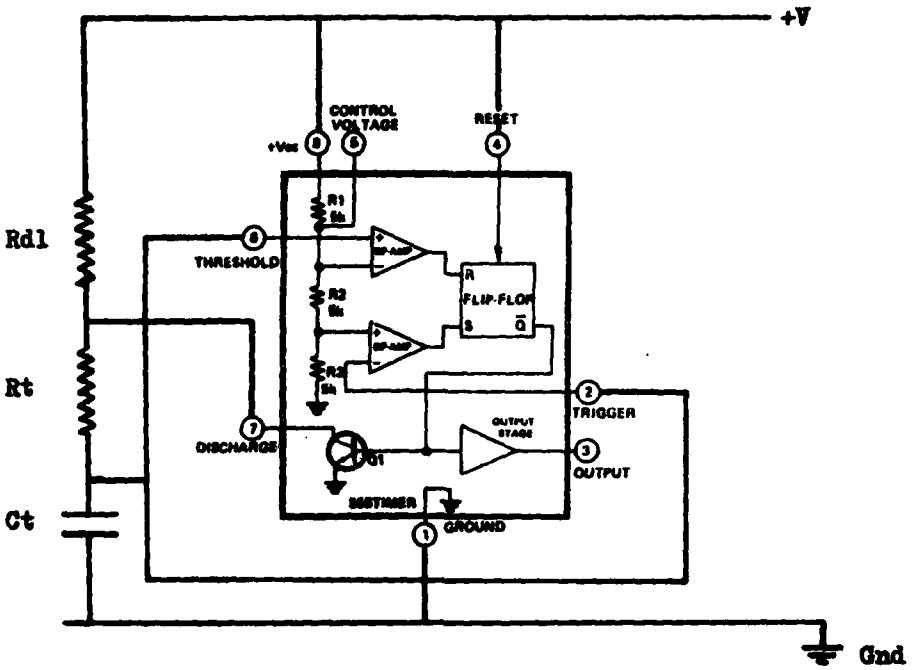
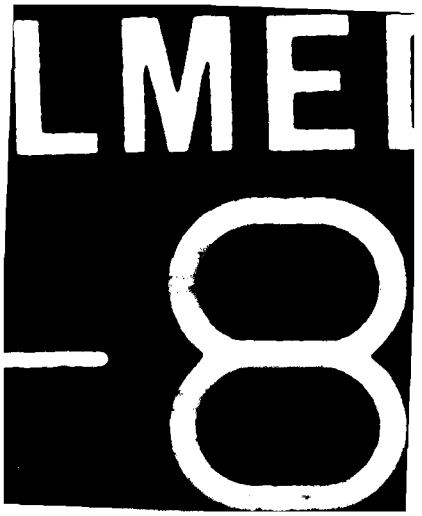


Figure A1. Functional block diagram of 555 timer.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